

REMARKS

Favorable reconsideration and allowance of the claims of the present application, as amended, is respectfully requested.

At the outset, in the present office action, the Examiner indicated that Claims 1-22 remain pending in this case; claims 23-30 being withdrawn.

In the present Office Action, the Examiner rejected Claims 1, 2, 4-10, 12-19, 21 and 22 were rejected under 35 U.S.C. 102(e) as being allegedly anticipated by Zhao et al. (US Patent Publication No. 2003/0105906) ("Zhao"). Claims 1, 2, 3 and 11 were further rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Gary et al. (US Patent No. 6,662,253) ("Gary"). Further in the Office Action, Claims 3, 11 and 20 were rejected under 35 U.S.C. 103(a) as allegedly unpatentable over Zhao in view of the reference to Ryu et al. entitled "A Comparison of Five Different Multi processor SoC Bus Architectures", Georgia Institute of Technology Electrical and Computer Engineering, Atlanta, GA ("Ryu")

The present invention is directed to multiprocessing devices generally and, particularly to a self-contained microprocessor subsystem for use in a system-on-chip (SoC) integrated circuit (IC) system that has a processing device (Core 440), a communications bus device and standardized components for enabling off-chip communications. As claimed in amended Claim 1, the self-contained microprocessor sub-system comprises:

a plurality of processor core assemblies, each processor core assembly comprising:

two or more microprocessor devices each capable of performing operations to implement a given processing functionality;

a storage device associated with said two or more microprocessor devices in said processor core assembly for storing at least one of data and instructions in said processor core assembly; and,

a first local interconnect means residing in each said processor core assembly for enabling communication of instructions and data between said two or more microprocessor devices; and,

a second local interconnect means for enabling communications between said plurality of processor core assemblies; and,

a bridging device implementing a common macro for enabling send and receive data communications between said second local interconnect means of said self-contained microprocessor sub-system and said SoC IC communications bus device, whereby said plurality of processor core assemblies may communicate with standardized components of said SoC IC via said bridging device, whereby self-contained microprocessor sub-system communications traffic is separated from communications traffic in said SoC without having to accommodate standardized components in said SOC system.

In view of the amendment to Claim 1, further amendments are being made to Claims 3, 4, 6 and 8-13 as submitted herein in order to conform these claims accordingly.

Respectfully, no new matter is being entered in amended Claim 1 as full support may be found in the specification, e.g., in Figures 5-8. For instance, as shown in Figure 7 and 8, the self-contained microprocessor subsystem (element 350) includes a plurality of processor core assemblies each comprising a quad 100' as shown in Figure 5 having two or more microprocessor devices (cores 125), interconnected by first local interconnect means for communicating instructions and data between said two or more microprocessor devices, a second local interconnect means (crossbar switch 120) and, a bridging device (element 410) implementing a common macro for enabling send and receive data communications (see description of Figure 8, paragraph [0048]).

Zhao respectfully does not teach nor suggest this self-contained microprocessor subsystem. Zhao provides no processor core assembly having the components including a bridging device (implementing a common macro) as claimed and thus, cannot be said to be anticipatory. In Zhao's configuration, moreover, communications traffic among the plurality of CPU/DSPs (element 10 in Zhao's Figure 1) is not separated from communications traffic in the SoC. This is because one of the processors (CPU/DSP 10) functions as the CPU core for the controlling the overall operation of a mobile station (Figure 9 of Zhao) and shares the same bus with every other CPU/DSP in the system (See paragraph [0045] of Zhao). This is contrary to the present invention as claimed in amended Claim 1 in that the SoC processor (e.g., the PPC 440 Core or like MIPS Core element 225 in Figure 7)) has its own processor local bus 210 (PLB) whereby the processor controls operation of the whole SoC device and communicates and operates in conjunction with standardized components for enabling communications providing traffic that is separated from communications traffic in the self-contained microprocessor subsystem (element 350) thereby avoiding bandwidth contention, unlike Zhao where all elements share the same bus.

This is a key difference between the Zhao and the self-contained microprocessor subsystem of the present invention.

Moreover, while the Zhao provides essentially data bus devices (program bus 12A, data bus 14A and control bus 16A in Figure 1 of Zhao), these are not likened to and are not suggestive of the three interconnect means as claimed in Claim 1, namely: the processor Quad bus (first local interconnect in each said processor core assembly for enabling communication of instructions and data); the switch fabric 120 (second local interconnect connecting the processor cores 100 to the bridge device;), and the SoC processor local bus

210 (communications bus device provided with the SoC). The prior art does not appear to teach any of these.

Moreover with respect to the rejection of Claims 9 and 10, Zhao does not teach or suggest the provision of the bridging device implementing a common macro that is selected to enable data flow between the processor based subsystem and the SoC bus, and particularly one that adapts communications signals and signaling protocols between two communication systems. As stated in the Office Action, the Examiner alleges the elements 15 and 17 in Figure 1 as suggestive of the claimed bridging device PLB macro. However, applicants respectfully disagree: Zhao's memory control unit element 15 in Zhao is a conventional DMA memory access device while the control unit 17 is a bus control unit. Neither elements 15 or 17 in Zhao teach or suggest a bridging device that adapts for different speeds, data widths, signals and signaling protocols between two communication systems as in the present invention.

Respectfully, Zhao's embodiment is quite different from the present invention as claimed in Claim 1. As such, the Examiner is respectfully requested to withdraw the rejection of independent Claim 1 under 35 U.S.C. 102(e) as being anticipated by Zhao.

Moreover, with respect to the rejection of Claims 3, 11 and 20, as these claims are dependent upon Claim 1, the novelty of which has now been demonstrated herein, applicants respectfully request that the Examiner withdraw the rejection of these claims based on the combination of Zhao and Ryu.

With respect to the rejection of Claim 14, Claim 14 of the present application has been similarly amended as in Claim 1 to set forth an SoC network processor architecture including an independent, self-contained multiprocessor subsystem core comprising:

- i) at least one microprocessor implementing a given functionality;

- ii) at least one memory storage device for storing at least one of data and instructions;
- iii) local interconnect means for enabling high-speed communication between two or more microprocessor devices, and,
- iv) a bridging device implementing a common macro for enabling send and receive data communications between said local interconnect means of said self-contained microprocessor sub-system and said SoC local system bus device,

wherein the independent, self-contained multiprocessor subsystem core provides multi-threading network processing capability.

In view of the amendment to Claim 14, further amendments are being made to Claims 15 and 22 in order to conform these claims with antecedents provided in amended Claim 14.

The arguments presented herein with respect to Claim 1 are further applicable and repeated herein with respect to Claim 14 and in view of the arguments presented, Zhao's embodiment neither teaches nor suggests an SoC network processor architecture including an independent, self-contained multiprocessor subsystem core as claimed in Claim 14. As such, the Examiner is respectfully requested to withdraw the rejection of independent Claim 14 under 35 U.S.C. 102(e) as being anticipated by Zhao.

With respect to the rejection of Claims 1-3 and 11 as being anticipated by Gary, applicants respectfully disagree. Gary, while suggestive of an embedded processor core, is non-analogous as being directed to different application, with no teaching or suggestion of:

a plurality of processor core assemblies, each processor core assembly comprising: